## **CLAIMS**

What is claimed is:

| 1 | 1.             | A series connected buck-boost regulator comprising:                     |
|---|----------------|---|
| 2 | a con          | trol circuit;   |
| 3 | a swi          | tching circuit for connecting to a source voltage;                      |
| 4 | an ou          | tput circuit connected to said switching circuit and for outputting a   |
| 5 |                | load voltage, wherein   |
| 6 | said o         | control circuit controls said output circuit and said input circuit for |
| 7 |                | operating said regulator in a plurality modes including:                |
| 8 |                | a current limiting (CL) mode;   |
| 9 |                | a buck mode; and  |
| 0 |                | a boost mode,   |
| 1 | where          | ein only a fraction of an output power of said regulator is switched    |
| 2 |                | by said switching circuit during one or both of the buck and the        |
| 3 |                | boost modes.  |
|   |                |   |
| 1 | 2.             | The regulator of claim 1 further comprising a transformer having        |
| 2 | a primary w    | inding and a center-tapped secondary winding, wherein the center        |
| 3 | tap of said s  | secondary winding is for connecting to the source voltage, and          |
| 4 | wherein said   | d primary winding is connected to said switching circuit, and           |
| 5 | further wher   | rein said secondary winding is connected to said output circuit.        |
|   |                |   |
| 1 | 3.             | The regulator of claim 1, wherein said switching circuit includes       |
| 2 | a first switch | n, a second switch, a third switch, and a fourth switch in a bridge     |
| 3 | configuratio   | n, and further wherein said output circuit includes a series            |
| 4 | connected f    | ifth and sixth switch connected to a series connected seventh and       |
| 5 | eighth switch  | ch.   |
|   |                |   |
| 1 | 4.             | The regulator of claim 3, wherein, during said boost mode, said         |
| 2 | control circu  | uit continuously turns on said fifth switch and said sixth switch, and  |

| 3  | further wherein said control circuit cycles through a plurality of boost states  |
|----|--|
| 4  | including:   |
| 5  | a first boost state wherein the first, fourth, and seventh switches are or       |
| 6  | and further wherein the second, third, and eighth switches are                   |
| 7  | off;   |
| 8  | a second boost state wherein the seventh and eighth switches are on,             |
| 9  | and further wherein the first, second, third, and fourth switches                |
| 0  | are off; and   |
| 11 | a third boost state wherein the second, third and eighth switches are o          |
| 12 | and further wherein the first, fourth, and seventh switches are                  |
| 13 | off.   |
| 1  | 5. The regulator of claim 3, wherein, during said buck mode, said                |
| 2  | control circuit continuously turns on said seventh switch and said eighth        |
| 3  | switch, and further wherein said control circuit cycles through a plurality of   |
| 4  | buck states including:   |
| 5  | a first buck state wherein said first, fourth, and sixth switches are on         |
| 6  | and further wherein said second, third, and fifth switches are off               |
| 7  | a second buck state wherein said fifth and sixth switches are on, and            |
| 8  | further wherein said first, second, third, and fourth switches are               |
| 9  | off; and   |
| 10 | a third buck state wherein said second, third, and fifth switches are on         |
| 11 | and further wherein said first, fourth, and sixth switches are off.              |
| 1  | 6. The regulator of claim 3, wherein, during said current limiting               |
| 2  | mode, said control circuit continuously turns off said first, second, third, and |
| 3  | fourth switches, and further wherein said control circuit cycles through a       |
| 4  | plurality of CL states including:  |
| 5  | a first CL state wherein said fifth, sixth, seventh, and eighth switches         |
| 6  | are on; and  |
| 7  | a second CL state wherein said fifth, sixth, seventh, and eighth                 |
| 8  | switches are off.  |

| 1  | <ol><li>The regulator of claim 3, further comprising a ninth</li></ol> | switch           |
|----|--|------------------|
| 2  | connected to said secondary winding which is turned off by said        | control circuit  |
| 3  | during said boost and said buck modes, but is turned on during         | said             |
| 4  | CURRENT LIMITING mode to short out said secondary winding              | •                |
|    |  |                  |
| 1  | 8. The regulator of claim 3, wherein each switch has                   | a diode          |
| 2  | placed in parallel.  |                  |
| 1  | 9. The regulator of claim 8, further comprising:                       |                  |
| 2  | a ninth switch connected to said center tap of said second             | dary winding     |
| 3  | which is turned off by said control circuit during sai                 | d boost and      |
| 4  | said buck modes, but is turned on during said CUF                      | RENT             |
| 5  | LIMITING mode to short out said secondary windir                       | ng;              |
| 6  | a freewheeling diode connected between said output circ                | uit and a        |
| 7  | ground;  |                  |
| 8  | a first transformer diode connecting a terminal of said sec            | condary to       |
| 9  | said ninth switch;   |                  |
| 10 | a second transformer diode connecting another terminal                 | of said          |
| 11 | secondary to said ninth switch; and                                    |                  |
| 12 | an inductor for connecting said output circuit to a load.              |                  |
| 1  | 10. The regulator of claim 9, wherein, during said boos                | st mode, said    |
| 2  | control circuit continuously turns on said fifth switch and said six   | th switch, and   |
| 3  | continuously turns off said ninth switch, and further wherein said     | l control circui |
| 4  | cycles through a plurality of boost states including:                  |                  |
| 5  | a first boost state wherein the first, fourth, and sev                 | enth switches    |
| 6  | are on and further wherein the second, third                           | d, and eighth    |
| 7  | switches are off;  |                  |
| 8  | a second boost state wherein the seventh and eight                     | hth switches     |
| 9  | are on, and further wherein the first, second                          | l, third, and    |

fourth switches are off; and

| 11 |              | a third boost state wherein the second, third and eighth switches     |
|----|--------------|---|
| 12 |              | are on and further wherein the first, fourth, and seventh             |
| 13 |              | switches are off;   |
| 14 | and w        | herein, during said buck mode, said control circuit continuously      |
| 15 |              | turns on said seventh switch and said eighth switch, and              |
| 16 |              | continuously turns off said ninth switch, and further wherein said    |
| 17 |              | control circuit cycles through a plurality of buck states including:  |
| 18 |              | a first buck state wherein said first, fourth, and sixth switches are |
| 19 |              | on and further wherein said second, third, and fifth                  |
| 20 |              | switches are off;   |
| 21 |              | a second buck state wherein said fifth and sixth switches are on,     |
| 22 |              | and further wherein said first, second, third, and fourth             |
| 23 |              | switches are off; and   |
| 24 |              | a third buck state wherein said second, third, and fifth switches     |
| 25 |              | are on, and further wherein said first, fourth, and sixth             |
| 26 |              | switches are off;   |
| 27 | and f        | urther wherein, during said CURRENT LIMITING mode, said               |
| 28 |              | control circuit continuously turns off said first, second, third, and |
| 29 |              | fourth switches, and continuously turns on said ninth switch, and     |
| 30 |              | further wherein said control circuit cycles through a plurality of    |
| 31 |              | CL states including:  |
| 32 |              | a first CL state wherein said fifth, sixth, seventh, and eighth       |
| 33 |              | switches are on; and  |
| 34 | a sec        | ond CL state wherein said fifth, sixth, seventh, and eighth           |
| 35 |              | switches are off.   |
|    |              |   |
| 1  | 11.          | The regulator of claim 1, further comprising a transformer having     |
| 2  | a primary w  | nding and a center-tapped secondary winding, with the center tap      |
| 3  | for connecti | ng to the source voltage, wherein                                     |
| 4  | said         | switching circuit includes a first switch, a second switch, a third   |
| 5  |              | switch, and a fourth switch in a bridge configuration, said           |

| 6   | primary w          | riding of said transformer connected to a center of         |
|-----|--------------------|---|
| 7   | said bridg         | e, and further wherein                                      |
| 8   | said output circui | t includes a series connected fifth and sixth switch        |
| 9   | connected          | to a terminal of said secondary winding and                 |
| 0   | connected          | to a series connected seventh and eighth switch             |
| l 1 | connected          | to another terminal of said secondary winding, and          |
| 12  | also where         | ein   |
| 13  | a ninth switch is  | included in said regulator for shorting out said            |
| 14  | transform          | er secondary winding on command from said control           |
| 15  | circuit.           |   |
| _   | 40 75              | . L C L. i  |
| 1   | _                  | ator of claim 11, wherein, during said boost mode, said     |
| 2   |                    | isly turns on said fifth switch and said sixth switch, and  |
| 3   | •                  | aid ninth switch, and further wherein said control circuit  |
| 4   |                    | ty of boost states including:                               |
| 5   |                    | st state wherein the first, fourth, and seventh switches    |
| 6   | are                | e on and further wherein the second, third, and eighth      |
| 7   | sw                 | itches are off;   |
| 8   | a second           | boost state wherein the seventh and eighth switches         |
| 9   | are                | on, and further wherein the first, second, third, and       |
| 10  | fou                | irth switches are off; and                                  |
| 11  | a third bo         | ost state wherein the second, third and eighth switches     |
| 12  | are                | e on and further wherein the first, fourth, and seventh     |
| 13  | sw                 | itches are off;   |
| 14  | and wherein, du    | ring said buck mode, said control circuit continuously      |
| 15  | turns on s         | said seventh switch and said eighth switch, and             |
| 16  | continuou          | ısly turns off said ninth switch, and further wherein said  |
| 17  | control ci         | rcuit cycles through a plurality of buck states including:  |
| 18  | a first bud        | ck state wherein said first, fourth, and sixth switches are |
| 19  | on                 | and further wherein said second, third, and fifth           |
| 20  | SW                 | ritches are off:  |

| 21 | a second buck state wherein said fifth and sixth switches are on,           |
|----|---|
| 22 | and further wherein said first, second, third, and fourth                   |
| 23 | switches are off; and   |
| 24 | a third buck state wherein said second, third, and fifth switches           |
| 25 | are on, and further wherein said first, fourth, and sixth                   |
| 26 | switches are off;   |
| 27 | and further wherein, during said CURRENT LIMITING mode, said                |
| 28 | control circuit continuously turns off said first, second, third, and       |
| 29 | fourth switches, and continuously turns on said ninth switch, and           |
| 30 | further wherein said control circuit cycles through a plurality of          |
| 31 | CL states including:  |
| 32 | a first CL state wherein said fifth, sixth, seventh, and eighth             |
| 33 | switches are on; and  |
| 34 | a second CL state wherein said fifth, sixth, seventh, and eighth            |
| 35 | switches are off.   |
| 1  | 13. A series connected buck-boost regulator comprising:                     |
| 2  | a control circuit;  |
| 3  | a transformer having a primary winding and a center-tapped secondary        |
| 4  | winding, wherein the center tap of said secondary winding is for            |
| 5  | connecting to a source voltage;   |
| 6  | a switching circuit controlled by said control circuit and for pulse-width- |
| 7  | modulating the source voltage for inputting into said primary               |
| 8  | winding, with said switching circuit including four PWM switches            |
| 9  | connected in a bridge configuration with said primary winding               |
| 10 | connected to a center of said bridge, wherein each PWM switch               |
| 11 | has a diode connected in parallel; and                                      |
| 12 | an output circuit controlled by said control circuit and connected to said  |
| 13 | secondary winding for outputting a load voltage, with said output           |
| 14 | circuit having two pairs of two series connected output switches            |
| 15 | connected in parallel, wherein each output switch also has a                |
| 16 | diode connected in parallel.  |

14. The regulator of claim 13, wherein said control circuit controls a duty cycle of said pulse-width-modulation of the source voltage and also drives said output circuit such that said output voltage can be varied in a range from a minimum voltage less than the source voltage to a maximum voltage greater than the source voltage.

- 15. The regulator of claim 14, wherein some substantial fraction of the power input by the source voltage is not pulse-width-modulated by said switching circuit during one or more operating modes.
- 16. The regulator of claim 15, wherein said PWM switches include a first switch, a second switch, a third switch, and a fourth switch, and further wherein said output switches include a fifth switch, a sixth switch, a seventh switch, and an eighth switch,

wherein, during said boost mode, said control circuit continuously turns on said fifth switch and said sixth switch, and further wherein said control circuit cycles through a plurality of boost states including:

- a first boost state wherein the first, fourth, and seventh switches are on and further wherein the second, third, and eighth switches are off;
- a second boost state wherein the seventh and eighth switches are on, and further wherein the first, second, third, and fourth switches are off; and
- a third boost state wherein the second, third and eighth switches are on and further wherein the first, fourth, and seventh switches are off;
- and wherein, during said buck mode, said control circuit continuously turns on said seventh switch and said eighth switch, and further wherein said control circuit cycles through a plurality of buck states including:

| 23 | on and further wherein said second, third, and fifth                            |    |
|----|---|----|
| 24 | switches are off;   |    |
| 25 | a second buck state wherein said fifth and sixth switches are on                | ١, |
| 26 | and further wherein said first, second, third, and fourth                       |    |
| 27 | switches are off; and   |    |
| 28 | a third buck state wherein said second, third, and fifth switches               |    |
| 29 | are on, and further wherein said first, fourth, and sixth                       |    |
| 30 | switches are off;   |    |
| 31 | and further wherein, during said current limiting mode, said control            |    |
| 32 | circuit continuously turns off said first, second, third, and fourth            |    |
| 33 | switches, and further wherein said control circuit cycles through               | 1  |
| 34 | a plurality of CL states including:   |    |
| 35 | a first CL state wherein said fifth, sixth, seventh, and eighth                 |    |
| 36 | switches are on; and  |    |
| 37 | a second CL state wherein said fifth, sixth, seventh, and eighth                |    |
| 38 | switches are off.   |    |
| 1  | 16. The regulator of claim 13, further comprising:                              |    |
| 2  | a first transformer diode connected to a terminal of said secondary             |    |
| 3  | winding;  |    |
| 4  | a second transformer diode connected to another terminal of said                |    |
| 5  | secondary winding; and  |    |
| 6  | a transformer shorting switch connected to said center tap of said              |    |
| 7  | secondary and also connected to said first and said second                      |    |
| 8  | transformer diodes for shorting said secondary on command                       |    |
| 9  | from said control circuit.  |    |
| 1  | 17. The regulator of claim 16, wherein said PWM switches include                | а  |
| 2  | first switch, a second switch, a third switch, and a fourth switch, and further |    |
| 3  | wherein said output switches include a fifth switch, a sixth switch, a seventh  |    |
| 4  | switch, and an eighth switch, wherein, during said boost mode,                  |    |

a first buck state wherein said first, fourth, and sixth switches are

| 5  | said control circuit continuously turns on said fifth switch and said sixth |
|----|---|
| 6  | switch, and continuously turns off said transformer shorting                |
| 7  | switch, and further wherein said control circuit cycles through a           |
| 8  | plurality of boost states including:  |
| 9  | a first boost state wherein the first, fourth, and seventh switches         |
| 10 | are on and further wherein the second, third, and eighth                    |
| 11 | switches are off;   |
| 12 | a second boost state wherein the seventh and eighth switches                |
| 13 | are on, and further wherein the first, second, third, and                   |
| 14 | fourth switches are off; and  |
| 15 | a third boost state wherein the second, third and eighth switches           |
| 16 | are on and further wherein the first, fourth, and seventh                   |
| 17 | switches are off;   |
| 18 | and wherein, during said buck mode, said control circuit continuously       |
| 19 | turns on said seventh switch and said eighth switch, and                    |
| 20 | continuously turns off said transformer shorting switch, and                |
| 21 | further wherein said control circuit cycles through a plurality of          |
| 22 | buck states including:  |
| 23 | a first buck state wherein said first, fourth, and sixth switches are       |
| 24 | on and further wherein said second, third, and fifth                        |
| 25 | switches are off;   |
| 26 | a second buck state wherein said fifth and sixth switches are on            |
| 27 | and further wherein said first, second, third, and fourth                   |
| 28 | switches are off; and   |
| 29 | a third buck state wherein said second, third, and fifth switches           |
| 30 | are on, and further wherein said first, fourth, and sixth                   |
| 31 | switches are off;   |
| 32 | and further wherein, during said current limiting mode, said control        |
| 33 | circuit continuously turns off said first, second, third, and fourth        |
| 34 | switches, and continuously turns on said transformer shorting               |
| 35 | switch, and further wherein said control circuit cycles through a           |
| 36 | plurality of CL states including:   |

| 37 | a first CL state wherein said fifth, sixth, seventh, and eighth  |
|----|--|
| 38 | switches are on; and   |
| 39 | a second CL state wherein said fifth, sixth, seventh, and eighth   |
| 40 | switches are off.  |
| _  | 40. The second star of eleies 47 further comprising:   |
| 1  | 18. The regulator of claim 17, further comprising:   |
| 2  | a freewheeling diode connected between said output circuit and a   |
| 3  | ground; and  |
| 4  | an inductor for connecting said output circuit to a load.  |
|    |  |
| 1  | <ol><li>The regulator of claim 18, wherein said control circuit controls a</li></ol>   |
| 2  | duty cycle of said pulse-width-modulation of the source voltage and also   |
| 3  | drives said output circuit such that said output voltage can be varied in a  |
| 4  | range from a minimum voltage less than the source voltage to a maximum   |
| 5  | voltage greater than the source voltage.   |
|    | and the state of t |
| 1  | 20. The regulator of claim 19, wherein some substantial fraction of  |
| 2  | the power input by the source voltage is not pulse-width-modulated by said   |
| 3  | switching circuit during one or more of said modes.  |